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Reduction of Leakage Power in Combinational Circuits

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Abstract: *Leakage power dissipation has become major portion of total power consumption in the integrated device and is expected to grow exponentially in the next decade as per International Technology Roadmap for Semiconductors (IRTS). This directly affects the battery operated devices as it has long idle times. Thus by scaling down the threshold voltage has tremendously increased the sub threshold leakage current thereby making the static power dissipation very high. To overcome this problem several techniques has been proposed to overcome this high leakage power dissipation. A comprehensive survey and analysis of various leakage power minimization techniques is presented in this paper. Of the available techniques, eight techniques are considered for the analysis namely, Multi Threshold CMOS (MTCMOS), Super Cut-off CMOS (SCCMOS), Forced Transistor Stacking (FTS) and Sleepy Stack (SS), Sleepy keeper (SK), Dual Stack (DS), and LECTOR. From the results, it is observed that Lector techniques produces lower power dissipation than the other techniques due to the ability of power gating.*

Keywords: *Sub-threshold leakage current, Threshold voltage, Transistor stacking, Low power, Deep submicron. LECTOR, Super Cut off, Forced Transistor Stacking*

I. Introduction

In order to achieve high density and high performance, CMOS technology feature size and threshold voltage have been scaling down for decades. Because of this technology trend, transistor leakage power has increased exponentially. As the feature size becomes smaller, shorter channel lengths result in increased subthreshold leakage current through a transistor when it is off. Low threshold voltage also results in increased subthreshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption, i.e., leakage power dissipation, has become a significant portion of total power consumption for current and future silicon technologies. There are several VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit the application of each technique. We propose a new approach, thus providing a new choice to low-leakage power VLSI designers. Previous techniques are summarized and compared with our new approach presented in this paper.

1.Subthreshold leakage current **(Isub)** in MOS transistors, which occurs when the gate voltage is below the threshold voltage and mainly, consists of diffusion current. Off-state leakage in present-day devices is usually dominated by this type of leakage. An effect called drain-induced barrier lowering (DIBL) takes place when a high-drain voltage is applied to a short channel device. The source injects carriers into the channel surface (independent of gate voltage). Narrow width of the transistor can also modulate the threshold voltage and the subthreshold current. where, μ0 is the zero bias mobility, Cox is the gate oxide capacitance, and (W/L) represents the width to the length ratio of the leaking MOS device. The variable V in equation 1.1 is the thermal voltage constant, and Vgs represents the gate to the source voltage. The parameter n in equation 1.1 is the sub-threshold swing coefficient given by 1 + (Cd/Cox) with Cd being the depletion layer capacitance of the source/drain junction. One important point about equation 1.1 is that the sub threshold leakage current is exponentially proportional to (Vgs-VT). Shorter channel length results in lower threshold voltages and increases subthreshold leakage. As temperature increases, subthreshold leakage is also increased. On the other hand, when the well-to-source junction of a MOSFET is reverse biased, there is a body effect that increases the threshold voltage and decreases subthreshold leakage.

$$Isub=\mu 0.Cox.W/L.V^2 .e^{1.8}\, e^{Vgs-Vt/\eta V} \quad \text{----------} \quad 1.1$$

2.*Gate oxide tunneling current* **(Igate)** in which tunneling of electrons that can result in leakage when there is a high electric field across a thin gate oxide layer. Electrons may tunnel into the conduction band of the oxide layer; this is called Fowler-Nordheim tunneling. In oxide layers less than 3-4 nm thick, there can also be direct tunneling through the silicon oxide layer. Mechanisms for direct tunneling include electron tunneling in the conduction band, electron tunneling in the valence band, and hole tunneling in the valence band

II. Different Basic Aproaches To Reduce Leakage Current

1. Sleep Mode Approach

We here review previously proposed circuit level approaches for subthreshold leakage power reduction. The most well-known traditional approach is the sleep approach [2][3]. In the sleep approach, both (i) an additional "sleep" PMOS transistor is placed between VDD and the pull-up network of a circuit and (ii) an additional "sleep" NMOS transistor is placed between the pull-down network and GND. These sleep transistors turn off the circuit by cutting off the power rails. Figure 1 shows its structure. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively. However, output will be floating after sleep mode, so the technique results in destruction of state plus a floating output voltage.

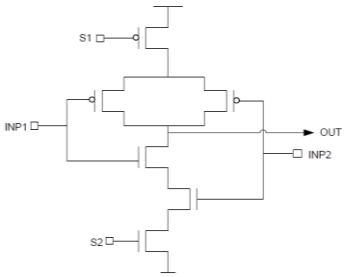

Fig.1. Sleep Approach NAND gate

2. Stack Approach

Another leakage power reduction technique is the stack approach, which forces a stack affect by breaking down an existing transistor into two half size transistors. Subthreshold leakage is exponentially related to the threshold voltage of the device, and the threshold voltage changes due to body effect [4]. From these two facts, one can reduce the subthreshold leakage in the device by stacking two or more transistors serially [5]. The transistors above the lowest transistor will experience a higher threshold voltage due to the difference in the voltage between the source and body as shown in Figure 2. Also, the Vds of the higher transistor is decreased, since the intermediate node has a voltage above the ground. These results in reduction of DIBL effect hence better leakage savings. However, forced stack devices have a strong performance degradation that must be taken into account when applying the technique [3-5].

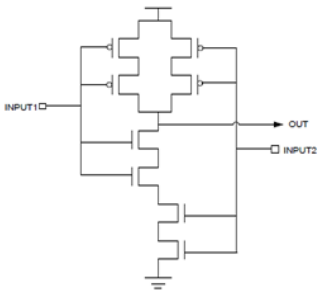

Fig. 2. Stack Approach based 2 input NAND gate

3.. Leakage Feedback Approach:

The leakage feedback approach is based on the sleep approach. However, the leakage feedback approach uses two additional transistors to maintain logic state during sleep mode, and the two transistors are driven by the output of an inverter which is driven by output of the circuit implemented utilizing leakage feedback [14].

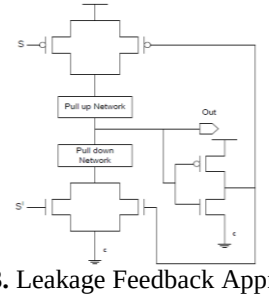

Fig.3. Leakage Feedback Approach

As shown in Figure 3, a PMOS transistor is placed in parallel to the sleep transistor (S) and a NMOS transistor is placed in parallel to the sleep transistor (S'). The two transistors are driven by the output of the inverter which is driven by the output of the circuit. During sleep mode, sleep transistors are turned off and one of the transistors in parallel to the sleep transistors keep the connection with the appropriate power rail.

4. Sleepy Stack Approach

The main idea behind the sleepy stack technique is to combine the sleep transistor approach during active mode with the stack approach during sleep mode. The structure of the sleepy stack approach is shown in Fig. 4. The sleepy stack technique divides existing transistors into two transistors each typically with the same width half the size of the original single transistor's width. Then sleep transistors are added in parallel to one of the transistors in each set of two stacked transistors; the divided transistors reduce leakage power using the stack effect while retaining state [5]. The sleepy stack technique divides existing transistors into two transistors each typically with the same width W1 half the size of the original single transistor's width (i.e.W1 = W0/2), thus, maintaining equivalent input capacitance. The added sleep transistors operate similar to the sleep transistors used in the sleep technique in which sleep transistors are turned on during active mode and turned off during sleep mode [6]. During active mode, *S*=0 and *S'*=1 are asserted, and thus all sleep transistors are turned on. Due to the added sleep transistor, the resistance through the activated (i.e., "on") path decreases, and the propagation delay decreases (compared to not adding sleep transistors while leaving the rest of the circuitry the same, i.e., with stacked transistors). During the sleep mode, *S*=1 and *S'*=0 are asserted, and so both of the sleep transistors are turned off. The stacked transistors in the sleepy stack approach suppress leakage current. Although the sleep transistors are turned off, the sleepy stack structure maintains exact logic state. The leakage reduction of the sleepy stack structure occurs in two ways. First, leakage power is suppressed by high- transistors, which are applied to the sleep transistors and the transistors parallel to the sleep transistors. Second, stacked and turned off transistors induce the stack effect which also suppresses leakage power consumption. By combining these two effects, the sleepy stack structure achieves ultra-low leakage power consumption during sleep mode while retaining exact logic state. The price for this, however, is increased area [4].

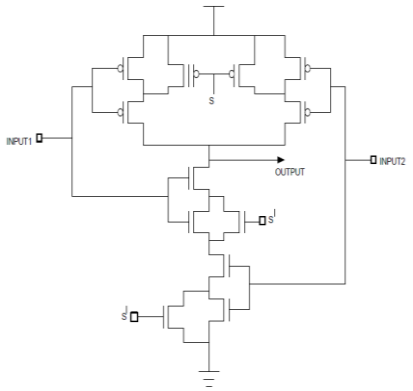

Fig. 4. Sleepy Stack Approach based 2 input NAND gate

An additional single NMOS transistor placed in parallel to the pull-up sleep transistor connects VDD to the pull-up network. When in sleep mode, this NMOS transistor is the only source of VDD to the pull-up network since the sleep transistor is off. Similarly, to maintain a value of „0" in sleep mode, given that the „0" value has already been calculated, the sleepy keeper approach uses this output value of „0" and a PMOS transistor connected to GND to maintain output value equal to „0" when in sleep mode. As shown in Figure 5, an additional single PMOS transistor placed in parallel to the pull-down sleep transistor is the only source of GND to the case pull-down network which is the dual case of the output „1" explained above [3]. For this approach to work, all that is needed is for the NMOS connected to VDD and the PMOS connected to GND to be able to maintain proper logic state[11]. This seems likely to be possible as other researchers have described ways to use far lower VDD values to maintain logic state.

III. Proposed Technique - Modified Lector Technique

In LECTOR technique two leakage control transistors (one p-type and one n-type) are introduced between pull-up and pull-down circuit within the logic gate for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other. This arrangement ensures that one of the LCTs always operates in its near cutoff region. The basic idea behind LECTOR approach is that "a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF

in any supply to ground path. When deep submicron transistor is operating in subthreshold region, the standby current varies exponentially with gate to source voltage. Most of the CMOS logic circuits are composed of series and parallel combination of MOS transistors. For parallel connected MOS transistors the DC current is calculated as the sum of the currents of each parallel connected transistor. In case of series connected transistors leakage current calculation is typical due to its nonlinear characteristics. In case of near cut off operation of transistors the resistance of transistor is as high as an OFF transistor's resistance but the available resistance is sufficient to increase the supply voltage to ground path resistance and so to reduce the leakage power dissipation.

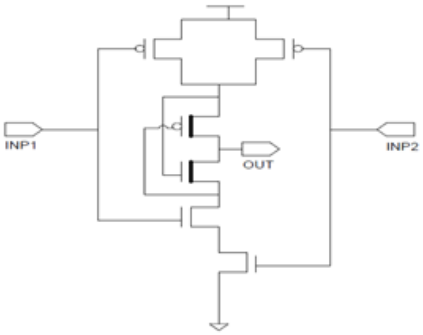

Fig. 5. Proposed technique Sleepy Lector with high Vth transistors

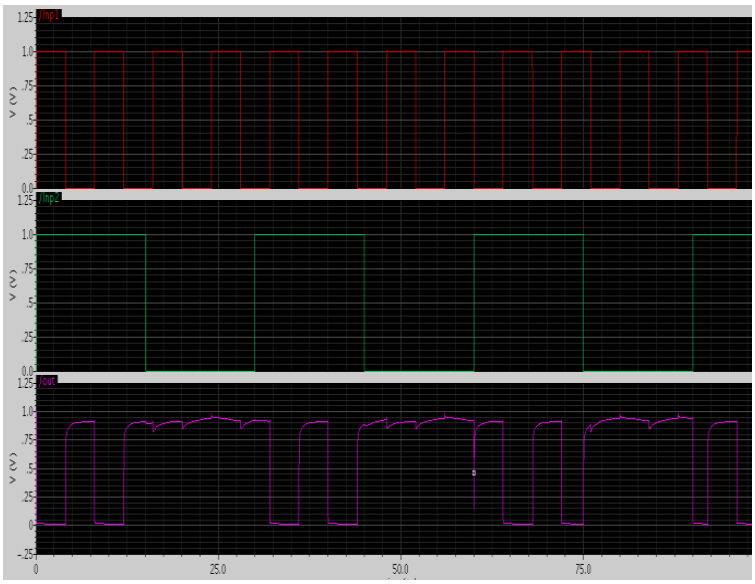

Fig.6. Output waveform of Lector with sleep

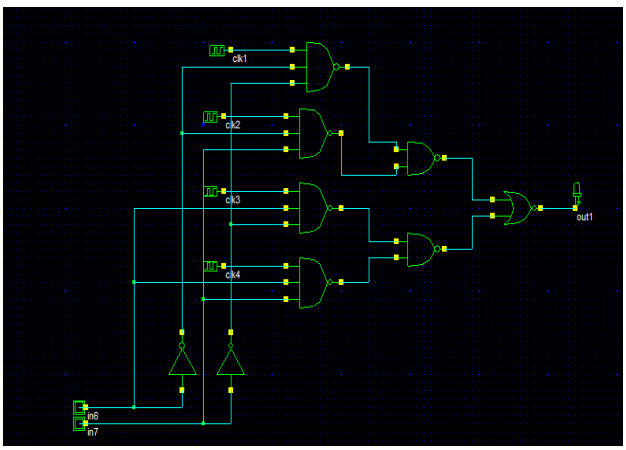

Fig 7. Proposed Lector With Multiplexer

Table: 1. Truth table of 4*1 MUX

A	B	Y			
0	**0**	**I0**	**0**	**0**	**0**
0	**1**	**0**	**I1**	**0**	**0**
1	**0**	**0**	**0**	**I2**	**0**
1	**1**	**0**	**0**	**0**	**I3**

IV. Simulation Results

A 2 input NAND gate is simulated with leakage power reduction techniques sleep, forced stack, sleepy keeper and sleepy stack with DTCMOS. After analyzing the results in terms of average power consumption, dynamic power consumption, static power consumption, delay and PDP we conclude that sleepy stack with DTCMOS is producing comparatively better results. All schematics are designed on Cadence virtuoso schematic editor and simulations are done on& Cadence spectre simulator on 65nm technology and supply voltage of 1V. The circuits are simulated with high threshold and low threshold NMOS and PMOS transistors.

Table 2. Average Power, delay & PDP Calculation of different Technique

Technique	Average Power(uW)	Delay(pS)	Power Delay Product(PDP)
Base case NAND Gate	1.532	3.70	5.66
Forced stacking	2.49	9.74	24.30
Sleep Transistor with Low Vth	1.25	6.91	8.68
NAND Gate with Lector	.749	.359	.2688
Proposed MUX with Lector	5.68	14.78	83.950

V. Conclusion

Leakage reduction technique plays a key role in VLSI circuit design. Scaling down the appropriate parameter can reduce the leakage power. It can be concluded that there is a strong correlation between three performance parameters: leakage power, delay, power delay product. There can be compromise in the performance metrics by reducing the other metric parameter. It can be concluded that SCCMOS provides efficient leakage power savings in standby and forced stacking modes. LECTOR method found more effective in both standby and active mode of operation. If propagation delay is taken as the performance metrics, then sleep transistor method is proved effective method in the standby mode. In active mode, sleepy stack based approach is suitable for faster circuit operation. All the above methods are suitable for circuit level of abstraction.

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